Remarks

Claims 1-20 are pending in the application. Claims 18-20 are newly added. Claims 1-17 stand rejected. Favorable reconsideration is respectfully requested.

The Applicant notes the Examiner's remarks in the Advisory Action mailed August 12, 2004, contending that the Ko reference meets the recitation "determining a level of sensitivity" as previously set forth in the Applicant's claims. While respectfully disagreeing with the Examiner's remarks, the Applicant has amended the claim language as set forth above to recite the feature in different terms, to highlight patentable differences between Ko and the claimed invention.

Notwithstanding the amendment of the claim language, as noted above, it is believed that the Examiner's remarks in the Advisory Action concerning the cited portions of Ko are inaccurate. The Examiner cites col. 8, lines 1-12 of Ko as support for the proposition that Ko teaches "determining a level of sensitivity" according to the claimed invention. The Applicant respectfully disagrees. As can be seen in Ko, col. 7, lines 59-67, Ko at col. 8, lines 1-12 is describing uniformly reducing frequency across a plurality of clocks in proportion to each clock's nominal frequency. That is, Ko describes in col. 7, lines 59-67 how a CPU 21 may include a number of functional units each driven by a clock with a different nominal frequency from that of other clocks. Then, the following passage at col. 8, lines 1-12 describes how each clock's frequency is uniformly reduced in proportion to its nominal frequency. For example, a 100 MHz clock's frequency is reduced to 50 MHz, and an 80 MHz clock's frequency is reduced to 40 MHz -- a 50% percent reduction for both.

Claims 1-17 were rejected under 35 USC 103(a) as being unpatentable over Georgiou et al. ("Georgiou") (US 5,940,785) in view of Ko (US 6,192,479).

Georgiou is silent as to a performance demanding level input to determine a rate of frequency reduction, as recited in each of independent claims 1, 7 and

12. Georgiou only discloses applying pre-determined voltage/frequency pairs, selected, based on temperature thresholds, to satisfy "critical timing paths" of a particular chip design. Specifically, for example, there is no input in Georgiou to determine a *rate* of frequency reduction.

Ko does not remedy deficiencies in Georgiou. Ko does not suggest a performance demanding level input to determine a rate of frequency reduction as recited the present claims. Instead, Ko only shows a linear correspondence between a required performance and a clock frequency. See FIG. 5 of Ko, which shows that in Ko there is only one rate of frequency reduction -- that indicated by the slope of the line in FIG. 5. There is no suggestion that the slope -- and thus the rate of frequency reduction -- is sensitive or responsive to any factor. By contrast, in embodiments of the present invention, a rate of frequency reduction can be higher or lower. This feature is described in more detail in the present specification at page 7, line 8 to page 8, line 2. As described, if the PDL signal 311 is asserted, for example, the level of sensitivity for frequency reduction may be higher, thereby calling for a lower rate frequency reduction (e.g., 1/15 reduction from normal frequency). On the other hand, if the PDL signal 311 is not asserted, for example, the level of sensitivity for frequency reduction may be lower, thereby calling for a higher rate of frequency reduction (e.g., close to 50% reduction from normal frequency). The determination of the level of sensitivity for frequency reduction may be based, for example, on what kind of application is being executed.

In view of the foregoing, independent claims 1, 7 and 12 are allowable over Georgiou. Moreover, since the dependent claims incorporate the limitations of the independent claims, they are likewise allowable for at least the reasons discussed in connection with the independent claims. Withdrawal of the rejection of claims 1-17 is therefore respectfully requested.

New claims 18-20 are also allowable over the art of record. For example, along the lines discussed above, nothing in the art of record suggests

performance demanding level logic to output a signal taking on values that respectively permit a first rate of frequency reduction and a second rate of frequency reduction, the first rate of frequency reduction being higher than the second, as called for by claims 18-20.

In light of the above, Applicant respectfully submits that the present application is in all aspects in allowable condition, and earnestly solicits favorable reconsideration and early issuance of a Notice of Allowance.

The Examiner is invited to contact the undersigned at (202) 220-4323 to discuss any matter concerning this application. The Office is authorized to charge any fees under 37 C.F.R. 1.16 or 1.17 related to this communication to Deposit Account No. 11-0600.

Respectfully submitted,

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